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EXAMINER	
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ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/628,726	MARISETTY ET AL.
	Examiner	Art Unit
	Michael C. Maskulinski	2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 19 May 2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1-4 and 21-23 is/are allowed.

6)☒ Claim(s) 5-19 and 24-26 is/are rejected.

7)☒ Claim(s) 20 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 24-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 24 claims a recording medium on which a program is stored and variations thereof. These claims therefore are interpreted as recording a program per se. In order to overcome this rejection, language, specifically stating the claim, **must be** limited to a computer program stored on a computer recordable medium executing on a computer.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 5-16 and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Bowers, U.S. Patent 6,308,285 B1.

Referring to claim 5:

a. In column 3, lines 45-48, Bowers discloses that because the processors control the functioning of the system generally under the control of software programming, memory is coupled to the processors to store and to facilitate execution of these programs (non-volatile memory to store an error handling routine and an idle routine). Further, in column 4, lines 57-59, Bowers discloses

that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode (an error handling routine and idle routine).

b. In column 2, lines 60-62, Bowers discloses that after the failed processor is replaced all the processors are awakened and the computer is returned to normal operation without the need to reboot the computer (said error handling routine to permit a computer system to continue operating when an error is detected).

c. In column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs (a plurality of slave processors to execute the idle routine). Further, in Figure 1, Bowers discloses that the plurality of slave processors are included in the computer system.

d. In column 5, lines 2-3, Bowers discloses a controller (monarch processor included in the computer system) that generates a stop clock signal STPCLK# and a sleep signal SLP# (error handling routine to correct an error).

Referring to claim 6, in column 4, lines 57-65, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode. Specifically, the processor will be placed into an

ACPI "S2" sleep state. To achieve this result, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS (a system abstraction layer located in the non volatile memory wherein the system abstraction layer includes the error handling routine).

Referring to claim 7, in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (wherein the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state).

Referring to claim 8:

a. In Figure 2, Bowers discloses a multiprocessor computer system (a plurality of processors) and a PAL controller (a monarch processor).

b. In column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs. An interface between the signals generated by the controller and the processors so that there is a processor abstraction layer coupled to the plurality of processors is inherent to the system.

c. In column 4, lines 57-67 continued in column 5, line 1, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and

prepares to place the identified processor into a sleep mode. Specifically, the processor will be placed into an ACPI "S2" sleep state. To achieve this result, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS. The routine generates a "start" signal and delivers it to the controller via the bridge/memory controller. An interface between the _PTS routine and the controller so that there is a system abstraction layer coupled to the processor abstraction layer is inherent to the system.

d. In column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses a sleep state signal that is passed from the operating system to the processors (an interrupt signaling mechanism coupled to the processor abstraction layer, the system abstraction layer, and the operating system layer to initiate a rendezvous state). Further, in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (ending the rendezvous state).

e. In column 5, lines 2-9, Bowers discloses placing the processors in a sleep state and having a controller not in the sleep state (said rendezvous state being a state where all but one of said processors in said plurality of processors are idle).

Referring to claim 9, in column 3, lines 45-48, Bowers discloses that because the processors control the functioning of the system generally under the control of software programming, memory is coupled to the processors to store and to facilitate execution of these programs (the processor abstraction layer is located in the non volatile memory

and is executed by the plurality of processors, and the system abstraction layer is located in the non volatile memory and is executed by the plurality of processors). Further, in column 4, lines 40-42, Bowers discloses an operating system of the computer (the operating system layer is located in the system memory and executed by the plurality of processors).

Referring to claim 10, in column 4, lines 57-67 continued in column 5, line 1, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode. Specifically, the processor will be placed into an ACPI "S2" sleep state. To achieve this result, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS (error handling routine included in the system abstraction layer). The routine generates a "start" signal and delivers it to the controller (monarch processor) via the bridge/memory controller. Further, in column 5, lines 10-13, Bowers discloses that after the processors have been placed into the sleep state (rendezvous state), the controller delivers a reset signal RESET# to the processor being removed, followed by de-assertion of the PWRGOOD signal (the monarch processor executing an error handling routine included in the system abstraction layer upon initiation of the rendezvous state).

Referring to claim 11, in column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units

except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs (the processor abstraction layer includes a functional module for error handling).

Referring to claim 12:

a. In Figure 2, Bowers discloses a multiprocessor computer system (a plurality of processors).

b. In column 3, lines 45-48, Bowers discloses that because the processors control the functioning of the system generally under the control of software programming, memory is coupled to the processors to store and to facilitate execution of these programs (a processor abstraction layer is located in a non volatile memory coupled to the plurality of processors, and a system abstraction layer located in the non volatile memory).

c. Further, in column 4, lines 40-42, Bowers discloses an operating system of the computer (an operating system layer located in a system memory coupled to the plurality of processors).

d. In column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs. An interface between the signals

generated by the controller and the processors so that there is a processor abstraction layer coupled to the plurality of processors is inherent to the system.

e. In column 4, lines 57-67 continued in column 5, line 1, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode. Specifically, the processor will be placed into an ACPI "S2" sleep state. To achieve this result, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS. The routine generates a "start" signal and delivers it to the controller via the bridge/memory controller. An interface between the _PTS routine and the controller so that there is a system abstraction layer coupled to the processor abstraction layer is inherent to the system.

f. In column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses a sleep state signal that is passed from the operating system to the processors (an interrupt signaling mechanism coupled to the processor abstraction layer, the system abstraction layer, and the operating system layer for initiation of a rendezvous state to initiate a rendezvous state). Further, in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (ending the rendezvous state upon receiving a signal that error handling is completed).

g. In column 5, lines 2-9, Bowers discloses placing the processors in a sleep state and having a controller not in the sleep state (said rendezvous state being a state where all but one of said processors in said plurality of processors are idle).

Referring to claim 13, in column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses a sleep state signal that is passed from the operating system to the processors (wherein the signal from the operating system to end the rendezvous state is an interrupt).

Referring to claim 14, In column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses a sleep state signal that is passed from the operating system to the processors (the processor abstraction layer is capable of sending a signal to the system abstraction layer to enter the rendezvous state). Further, in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (performing error handling upon entering the rendezvous state).

Referring to claim 15:

a. In column 7, lines 1-4, Bowers discloses that if multiple processors are to be removed or replaced these processors may be identified by a failure detection system or by the user via a software or hardware interface (detecting an error by one processor included in a multiple processor system).

b. In column 5, lines 2-13, Bowers discloses placing the processors in a sleep state (entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle).

c. In column 5, lines 10-13, Bowers discloses that after the processors have been placed into the sleep state (rendezvous state), the controller delivers a reset signal RESET# to the processor being removed, followed by de-assertion of the PWRGOOD signal (correcting the error using the one processor).

d. In column 2, lines 60-62, Bowers discloses that after replacement of the processor, all processors are awakened and the computer is returned to normal operation without the need to reboot the computer (resuming normal operation).

Referring to claim 16, in column 5, lines 2-13, Bowers discloses placing the processors in a sleep state (requesting a plurality of processors included in the multiple processor system to enter an idle state) and that after the processors have been placed into the sleep state (waiting until the plurality of processors have entered the idle state), the controller delivers a reset signal RESET# to the processor being removed, followed by de-assertion of the PWRGOOD signal.

Referring to claim 24:

a. In column 5, lines 2-9, Bowers discloses placing the processors in a sleep state and having a controller not in the sleep state (attempting to correct an error by a detecting processor included in a multiple processor system).

b. In column 4, lines 60-62, Bowers discloses that the operating system services the SCI interrupt (error) by calling a _PTS routine stored in the ROM/BIOS (on failure, executing firmware code operatively coupled to all the processors included in the multiple processor system to correct the error).

c. In column 5, lines 2-9, Bowers discloses placing the processors in a sleep state and having a controller not in the sleep state (on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of said processors included in the multiple processor system are idle).

Referring to claim 25, in column 5, lines 2-9, Bowers discloses placing the processors in a sleep state (wherein all but the one of the processors included in the multiple processor system are executing a spin loop) and having a controller not in the sleep state.

Referring to claim 26, in column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit (informing a processor abstraction layer when all but one of the processors included in the multiple processor system have entered the idle state).

5. Claims 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al., U.S. Patent 6,065,078.

Referring to claim 18:

a. In column 1, lines 34-48, Falik et al. disclose that the debugger interface sends a debugger command to at least one of the plurality of processors (attempting to correct an error by a detecting processor included in a multiple processor system).

b. In column 4, lines 41-47, Falik et al. disclose sending an interrupt to a processor, which stops the execution of the application program and starts to execute the monitor (on failure, executing firmware code operatively coupled to all the processors included in the multiple processor system to correct the error).

c. In column 7, lines 26-30, Falik et al. disclose that the interrupt control module issues an ISE interrupt request to either a specific one of the processors or to multiple processors (on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle).

Referring to claim 19:

a. The debugger interface of Falik et al. is pre-designated making it the monarch processor from the processors included in the multiple processor system.

b. In column 4, lines 41-47, Falik et al. disclose sending an interrupt to a processor, which stops the execution of the application program (signaling slave processors included in the multiple processor system to execute a spin loop) and starts to execute the monitor (correcting the error by the monarch processor).

d. In column 2, lines 43-46, Falik et al. disclose that after the phase of debugging software for the processors of the multiprocessor integrated circuit, the multiprocessor integrated circuit would, in most cases, no longer interact with the host computer (resuming normal operation by the plurality of processors).

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bowers, U.S. Patent 6,308,285 B1, and further in view of Fujii et al., U.S. Patent 5,892,898. In column 2, lines 49-62, Bowers discloses removing or replacing one or more of the processors for various reasons. However, Bowers doesn't explicitly disclose determining if the error is a severe error and only upon determining that the error is a severe error, entering the rendezvous state. In column 2, lines 14-19, Fujii et al. disclose an event message that corresponds to an event type that includes at least one event type selected from the group consisting of an information event type, a warning event type, and an error event type. It would have been obvious to one of ordinary skill at the time of the invention to include the event categorizing method of Fujii et al. into the system of Bowers. A person of ordinary skill in the art would have been motivated to make the modification because an error event type is used to report a non-recoverable problem (see Fujii et al.: col.2, lines 62-63) and a warning event type is used to indicate some kind of recoverable anomaly (see Fujii et al.: col. 2, lines 60-62). Knowing the severity determines what action should be taken (removal of a processor) (see Fujii et al.: col. 2, lines 48-55).

Allowable Subject Matter

8. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 1-4 and 21-23 are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter:

Referring to claims 21-23, the prior art does not teach or reasonably suggest executing a spin loop routine in a second firmware layer by the plurality of processors except the monarch processor and accessing a routine in the second firmware layer to correct the error.

Referring to claims 1-5, the prior art does not teach or reasonably suggest that each processor of the plurality is capable of accessing the error handling routine on detecting an error and signaling remaining processors of the plurality to enter a rendezvous state.

Response to Arguments

11. Applicant's arguments filed May 19, 2005 have been fully considered but they are not persuasive.

12. On page 8, under the section *101 Rejection of the Claims,* the Applicant argues, "These claims are therefore directed to an article of manufacture, including a system 500 executing code stored in a system memory 540, and as such, constitute patentable subject matter." The Examiner respectfully disagrees. A system and executable code may be an article of manufacture and a machine, but it is not necessarily true vice

versa. A machine is not always a computer and a machine-accessible medium can be a piece of paper being scanned. The Applicant has referred to *Alappat,* which is concerned with a computer not a machine. It appears that the Applicant is trying to claim a computer readable medium storing instructions that are executed by a computer, and the Examiner requests that the Applicant amends the claims to such.

13. On pages 9 and 11, the Applicants indicate that "the Applicants do not admit that Bowers or Falik or Fujii are prior art, and reserve the right to swear behind these references in the future." The Examiner would like to note that any affidavit filed after this response will not be considered timely filed and will not be entered.

14. Applicant's arguments on pages 9-10, with respect to claim 1 have been fully considered and are persuasive. The rejection of claims 1-4 has been withdrawn.

15. On page 10, under the section *102 Rejection of the Claims*, the Applicant argues, "Bowers also does not teach or suggest a 'monarch processor being capable of executing the error handling routine to correct the error...' as claimed by the Applicants in independent claim 5 such that 'the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state' as claimed in claim 7." The Examiner respectfully disagrees for at least the reasons given in the rejection above. Further, the Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

16. On page 10, under the section *102 Rejection of the Claims*, the Applicant argues, "Bowers does not teach or suggest 'a plurality of processors including a monarch processor ... and an interrupt signaling mechanism ... to initiate a rendezvous state ... being a state where all of the plurality of processors but the monarch processor are idle' as claimed by the Applicants in independent claim 8 (and dependent claims 9-11). In addition, Bowers does not teach or suggest 'a plurality of processors ... and an operating system layer ... to signal all but one of the plurality of processors to end a rendezvous state ... upon receiving a signal that error handling is completed, said rendezvous state being a state wherein all but the one of said plurality of processors are idle' as claimed by the Applicants in independent claim 12 (and dependent claims 13-15)." The Examiner respectfully disagrees for at least the reasons given in the rejection above. Further, the Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

17. On page 10, under the section *102 Rejection of the Claims*, the Applicant argues, "Bowers also does not teach or suggest 'detecting an error ...; entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle; ... and ... correcting the error using the one processor' as claimed by the Applicants in independent claim 15 (and dependent claims 16-17). Finally, Bowers does not teach or suggest 'attempting to correct an error ... in a multiple processor system ... and on failure, entering a rendezvous state to correct the error, said

rendezvous state being a state where all but one of the processors included in the multiple processor system are idle' as claimed by the Applicants in claim 24 (and dependent claims 25-26)." The Examiner respectfully disagrees for at least the reasons given in the rejection above. Further, the Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

18. On pages 10-11, under the section *102 Rejection of the Claims*, the Applicant argues, "Falik suffers from similar deficiencies. Specifically, Falik fails to disclose 'attempting to correct an error by a detecting processor included in a multiple processor system' and 'entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle' as claimed in claims 18 and 19. While the Office Action asserts that Falik's debugger interface is somehow equivalent to a 'detecting processor included in a multiple processor system', this does not comport with the clear distinction Falik makes between the host computer 1820 and the multiprocessor integrated circuit 1810." The Examiner respectfully disagrees for at least the reasons given in the rejection above. The Examiner is unsure as to what the Applicant means by "this does not comport with the clear distinction Falik makes between the host computer 1820 and the multiprocessor integrated circuit 1810." The Examiner has shown in the rejection what elements of Falik are equivalent to the Applicant's claimed elements and is unsure as to what this distinction has to do with anything.

19. On page 11, under the section *102 Rejection of the Claims*, the Applicant argues, "Even if it is assumed that Falik's debugger can operate as a 'detecting processor' how does Falik's system correct the error? Falik's debugger, or a monitor, are the only resources available, and neither one operates to 'correct' the error. It is respectfully noted that the term "error" appears only once in Falik, concerning bus communication error probability. However, such errors are not processed by Falik's system. See Falik, Col. 18, lines 31-32. In fact, Falik states that, while such errors can be cured by a system reset, such operation should be 'avoided by the host' since this resets the entire chip. See Falik, Col, 18, lines 39-47." The Examiner respectfully disagrees. First of all, the Examiner would like to note that the number of times the word error occurs in a reference is an ineffective way to show whether or not errors are present and corrected. The word error has numerous synonyms such as problem, malfunction, fault, and failure. Further, it is noted that Falik is concerned with a debugger. To debug by definition is "to detect, locate, and **correct** logical or syntactical **errors** in a program or **malfunction** in hardware."[1] In column 2, lines 43-46, Falik et al. disclose that the debugging phase completed, therefore, the error was corrected.

20. On page 11, under the section *102 Rejection of the Claims*, the Applicant argues, "Finally, how can 'all but one of the processors included in the multiple processor system' be idle, as asserted in the Office Action, if at least one processor in the multiprocessor integrated circuit 1810 must be awake to execute a monitor, *in addition* (emphasis by Applicant) to the debugger of Falik's host computer? The debugger

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[1] Microsoft Computer Dictionary, Fifth Edition, 2002, page 148.

communicates with the monitor on one of the processors, which means at least two processors must be operational in Falik's system. See Falik, Col. 17, lines 27-46." The Examiner respectfully disagrees. The Examiner has examined Falik, col. 17, lines 27-46 and is unsure as to where the Applicant gets the notion that at least two processors must be operational. Further, in column 7, lines 26-30, Falik et al. disclose that the interrupt control module issues an ISE interrupt request to either a specific one of the processors or to multiple processors (on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle).

21. On page 11, under the section *103 Rejection of the Claims*, the Applicant argues, "First there is no motivation to combine Bowers and Fujii. Bowers never uses the term 'error', or discloses any type of error detection or handling routine. Processor boards are simply replaced after the fact – notably, for routine maintenance. Similarly, Fujii never mentions removing a processor from a system." The Examiner respectfully disagrees. The Examiner would like to note once again that the number of times the word error appears in a reference is an ineffective way to show that errors did or didn't occur. To replace a processor for routine maintenance indicates that there is something wrong with the processor and that it was causing errors as shown in Bowers: column 1, lines 66-67 continued in column 2, lines 1-11. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or

motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, an error event type is used to report a non-recoverable problem (see Fujii et al.: col.2, lines 62-63) and a warning event type is used to indicate some kind of recoverable anomaly (see Fujii et al.: col. 2, lines 60-62). Knowing the severity determines what action should be taken (removal of a processor) (see Fujii et al.: col. 2, lines 48-55).

22. On pages 11-12, under the section *103 Rejection of the Claims*, the Applicant argues, "Second the Office mischaracterizes the claimed 'severe error' (which causes entry into a rendezvous state) as a 'non-recoverable problem' documented by Fujii. However, this characterization does not comport with the concept of a 'rendezvous state' claimed by the Applicants." The Examiner respectfully disagrees. It is noted that the features upon which applicant relies (i.e., Application page 7, lines 19-24) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claim 17 fails to mention that the error is recoverable or non-recoverable, but rather, refers to the error as being severe. A non-recoverable error is severe. For this reason it is reasonable for the Examiner to interpret it as such.

23. On page 12, under the section *103 Rejection of the Claims*, the Applicant argues, "Third, it is not necessarily true that 'knowing the severity of the event determines what

action should be taken (e.g., removal of a processor)' as asserted in the Office Action. Errors of varying severity can occur within a computer system, and knowledge of the severity (e.g., non-recoverable) will not always be determinative as to whether a processor should be replaced (e.g. a main memory failure may be the culprit, or a hard disk failure, etc.). Since there is no evidence in the record to support the Office Action assertion, the explicit requirements set forth by *In re Sang Su Lee* are not satisfied." The Examiner respectfully disagrees. The primary reference of Bowers is concerned with replacing processors and only that. Therefore, any error detected in Bowers is concerned with just the processors. Bowers is silent as to how it is determined if the processor should be replaced. Fujii cures this deficiency by relating the severity of errors with appropriate actions. The Examiner doesn't rely on personal knowledge, but rather what is taught by each reference.

24. On page 12, under the section *103 Rejection of the Claims*, the Applicant argues, "Fourth, it should be noted that neither Bowers nor Fujii disclose using a processor that is part of a multi-processor system to correct an error within the system, as claimed by the Applicants." The Examiner respectfully disagrees for at least the reasons given in the rejection above.

25. On pages 12-13, under the section *103 Rejection of the Claims*, the Applicant argues, "Fifth, combining Bowers with Fujii gives no reasonable expectation of success. Fujii merely teaches the existence of an error recording system, not a system to correct errors. The mechanism of replacing a processor (as taught by Bowers) in response to recording non-recoverable errors, advocated in the Office Action, also may not have any

effect on solving the actual problem (e.g., a main memory failure, or a cache failure)." The Examiner respectfully disagrees for at least the reasons given in paragraph 23 above.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

SCOTT BADERMAN
PRIMARY EXAMINER